IN THE CLAIMS:

Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Please amend claims 1, 3, 4, 23 and 25 as set forth below.

Listing of Claims:

1. (Presently Amended) A method of forming an integrated circuit package, the method comprising:

forming a lead frame having a plurality of conductors and at least one alignment feature ~~electrically isolated from the plurality of conductors~~;

coupling at least some of the plurality of conductors to a semiconductor die;

encapsulating the semiconductor die and a portion of the lead frame with an insulating material;

electrically isolating the at least one alignment feature from the plurality of conductors subsequent the encapsulating the semiconductor die and a portion of the leadframe; and

removing the at least one alignment feature subsequent the ~~encapsulating the semiconductor die and a portion of the lead frame~~ electrically isolating the at least one alignment feature from the plurality of conductors.

2. (Canceled)

3. (Presently Amended) A method of forming an integrated circuit package, the method comprising:

forming a leadframe having ~~providing~~ a plurality of conductors and at least one alignment feature;

coupling at least some of the plurality of conductors to a semiconductor die; and

encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material; and

electrically isolating the at least one alignment feature from the plurality of conductors.

4. (Presently Amended) A method of forming and testing an integrated circuit package, the method comprising:

forming a leadframe having ~~providing~~ a plurality of conductors and at least one alignment feature;

electrically coupling at least some of the plurality of conductors to a semiconductor die;

encompassing the semiconductor die, a portion of each of the plurality of conductors, and substantially encompassing the at least one alignment feature with an insulating material;

electrically isolating the at least one alignment feature from the plurality of conductors;

coupling the at least one alignment feature encompassed by the insulating material with a portion of a testing device; and

testing the integrated circuit package through at least some of the electrically coupled conductors.

5-17. (Canceled)

18. (Original) The method according to claim 1, further comprising forming the at least one alignment feature to include at least one aperture.

19. (Original) The method according to claim 1, further comprising forming the at least one alignment feature to include a plurality of apertures.

20. (Original) The method according to claim 1, further comprising forming a separation line in the lead frame and wherein removing the at least one alignment feature further comprises removing the at least one alignment feature along the separation line.

21. (Original) The method according to claim 20, wherein the forming a separation line in the lead frame includes perforating the separation line.

22. (Original) The method according to claim 1, further comprising forming the at least one alignment feature to include a tab.

23. (Presently Amended) A method of forming and testing an integrated circuit package, the method comprising:

forming a lead frame having a plurality of conductors and at least one alignment feature ~~electrically isolated from the plurality of conductors~~;

coupling at least some of the plurality of conductors to a semiconductor die;

encapsulating the semiconductor die and a portion of the lead frame with an insulating material;

electrically isolating the at least one alignment feature from the plurality of conductors subsequent the encapsulating the semiconductor die and a portion of the lead frame with an insulating material;

coupling the at least one alignment feature with a portion of a testing device;

testing the integrated circuit package through at least some of the electrically coupled conductors;

decoupling the at least one alignment feature from the portion of the testing device; and

removing the at least one alignment feature subsequent the decoupling the at least one alignment feature from the portion of the testing device.

24. (Original) The method according to claim 3, further comprising forming the at least one alignment feature to include an alignment cut-out.

25. (Presently Amended) The method according to claim 3, further comprising ~~coupling~~ disposing a heat spreader adjacent to, and in contact with, an external surface of the insulating material and, forming at least one other alignment feature in the heat spreader.

26. (Original) The method according to claim 3, further comprising providing a tie bar and forming the at least one alignment feature in the tie bar.

IN THE DRAWINGS:

The attached sheet of drawings includes changes to FIG 4. (now labeled FIG. 4A) and new FIG. 4B. FIG. 4B is presented in response to the Examiner's objection to the drawings under 37 CFR 1.83(a).